## REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on June 7, 2006, and the references cited therewith.

### *Status of Claims*

New dependent claim 18 is added, and claims 1-18 are now pending in this application.

### *Double Patenting Rejection*

The provisional obviousness type double patenting rejection is stayed pending the outcome of co-pending application Serial No. 10/422,829. At that time, if the Examiner believes that the obviousness type double patenting rejection still applies, a terminal disclaimer will be discussed and considered.

### *35 USC §103 Rejection of the Claims*

Claims 1 – 3 and 7 – 8 were rejected under 35 USC § 103(a) as being unpatentable over Kobayashi (U.S. Patent No. 6,373,346) in view of Bosch et al. (U.S. Patent No. 6,130,562), and further in view of Inoue et al. (U.S. Patent No. 6,975,813). Applicants respectfully traverse this rejection.

Independent claim 1 recites a laser driver circuit comprising "a duty cycle control circuit, including an average power approximation circuit, to control the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal" (emphasis added). Independent method claim 7 similarly recites "controlling the duty cycle of the pulse data output signal based, at least in part, upon an approximation of the average power of the pulse data output signal." In one embodiment, for example, an input stage generates a differential signal on first and second terminals, and the duty cycle control circuit includes a current steering circuit to apply an offset current to at least one of first and second terminals, as recited in dependent claim 3. In a further embodiment, the average power approximation circuit is configured to maintain a voltage at an input terminal of the current steering circuit, which represents the approximation of the average power of the pulse data output signal, as recited in new dependent claim 18.

Kobayashi discloses a laser driver pre-emphasis and de-emphasis method and architecture with duty cycle control. As acknowledged in the Office Action, "Kobayashi does not teach the duty cycle to be based on an average power of the pulse data output signal, or to include an average power approximation circuit." The Office Action relies on Bosch and Inoue as allegedly teaching these features. Applicants respectfully disagree with the characterizations of Bosch and Inoue and submits that neither Bosch, nor Inoue, teach or suggest controlling a duty cycle of a pulse data output signal based, at least in part, on average power of the pulse data output signal.

Bosch discloses a digital driver circuit 100 including three stages – an input stage 112, 212, level shifting stage 130, 230, and an output stage 140, 240 (see FIGS. 2 and 3, col. 3, lines 32-34). An output amplitude control circuit 125, 225 provides an output used as a control voltage $V_{C2}$ of the input stage 112, 212 to automatically control and maintain the output voltage and current of the output stage 140, 240 (see col. 3, lines 46-50, col. 4, lines 8-11, and col. 5, lines 9-32). Bosch does not teach or suggest that the control voltage $V_{C2}$ be used to control duty cycle. The Office Action characterizes element 212 in FIG. 3 of Bosch as "a duty cycle circuit;" however, Bosch describes an input stage 212. Thus the "output feedback" mentioned in the Office Action is provided to the input stage 212, <u>not</u> a duty cycle control circuit, and what is being controlled is the output voltage, <u>not</u> a duty cycle of a pulse data output signal. Thus, Bosch does not teach controlling the duty cycle of a pulse data output signal based on the power of the pulse data output signal. Bosch merely teaches control of the output voltage and current to provide "increased output current and voltage amplitudes in a digital driver circuit" (see col. 2, lines 42-43).

In one embodiment in Bosch, a Mark-Bar reference voltage $V_{MBREF}$ is used to control the output voltage and current of the output stage 240. Bosch mentions that the Mark-Bar reference voltage is a DC voltage corresponding to the average duty cycle of the input data signals and further states that the value of the Mark-Bar reference voltage $V_{MBREF}$ is user defined (see col. 5, lines 9-32). Thus, Bosch merely refers to average duty cycle as it relates to a Mark-Bar reference voltage $V_{MBREF}$, but does not teach or suggest control of the duty cycle. The fact that the Mark-Bar reference voltage $V_{MBREF}$ corresponding to the average duty cycle of the input data

signals is user defined actually teaches away from the claimed invention, which controls duty cycle based on average power of the pulse data output signal.

The asserted teaching of Inoue does not remedy this deficiency in Bosch. The Office Action refers to the element 20 in FIG. 4 of Inoue as "an average power approximation circuit." According to Inoue, "[a] photodiode (PD) 18 produces a monitor current proportional to the amount of light emitted by the light-emitting device (LD), and a monitor section 20 converts the monitor current value into a voltage value and holds its peak value." Inoue further states "[w]ith this operation, the light output is controlled at a constant value with respect to the reference value, using negative feedback control." See Inoue, col. 1, lines 35-49. Thus, Inoue is controlling light output (<u>not</u> duty cycle) at a constant value by monitoring current proportional to the light output. Although the monitor section 20 "uses an average value detection circuit comprising a resistor and a capacitor," the average value is of the current proportional to the light output (as measured by photodiode 18). This proportional current is <u>not</u> a pulse data output signal. Thus, the teaching of Inoue is limited to the use of the monitor section 20 in Inoue to control light output based on an average value of a current proportional to the light output. Inoue does not teach or suggest controlling a duty cycle of a pulse data output signal based, at least in part, on average power of the pulse data output signal.

At best, a combination of Kobayashi, Bosch and Inoue might result in the output voltage and current of the laser driver in Kobayashi being controlled by providing feedback to an input stage of Kobayashi (i.e., control circuits 102, 104). However, neither Bosch, nor Inoue, taken alone or combined, suggest the desirability of modifying the duty cycle compensation control circuit 150 in Kobayashi such that duty cycle of the pulse data output signal is controlled based on, at least in part, an approximation of an average power of the pulse data output signal, as recited in independent claims 1 and 7.

Moreover, Kobayashi teaches away from such a modification that would result in the duty cycle compensation circuit 150 controlling the duty cycle based on an average power of the pulse data output signal. As described in the previous Amendments dated January 25, 2006 and September 26, 2005, Kobayashi teaches a laser driver circuit that may provide positive peak control or pre-emphasis (provided by circuit 102 of FIG. 2 or circuit 102' of FIG. 6) and negative peak control or de-emphasis (provided by circuit 104 of FIG. 2 or circuit 104' of FIG. 6). (see

col. 4, lines 19 – 21). The pre-emphasis and de-emphasis may introduce duty cycle distortion seen in Kobayashi's FIGs. 4a and 5a when compared to FIG. 3a (see col. 6, lines 42 – 44). Therefore, in the embodiment of FIG. 6, Kobayashi teaches a control circuit 150 "implemented as a duty cycle distortion (DCD) control circuit that compensates for the DC offset that may be introduced by the pre-emphasis and de-emphasis circuits 102 and 104" (see col. 6, lines 60 – 63). Thus, Kobayashi teaches away from duty cycle control based on average power of the pulse data output signal by teaching a duty cycle compensation circuit 150 that is provided to compensate for DC offset produced by the pre-emphasis and de-emphasis circuits 102' and 104'.

Because the combination of Kobayashi, Bosch and Inoue fails to teach or suggest all of the limitations recited in independent claims 1 and 7, applicants submit that this combination of references fails to establish *prima facie* obviousness with respect to claims 1 and 7 and the claims dependent therefrom. Accordingly, applicants request that the rejection of claims 1-3 and 7-8 under 35 U.S.C. 103 be withdrawn.

Claims 4 – 6 and 9 – 11 were rejected under 35 USC § 103(a) as being unpatentable over Kobayashi (U.S. Patent No. 6,373,346), Bosch et al. (U.S. Patent No. 6,130,562) and Inoue et al. (U.S. Patent No. 6,975,813), and further in view of Gilliland et al. (U.S. Patent No. 6,711,189). Claim 12 was rejected under 35 USC § 103(a) as being unpatentable over Kobayashi (U.S. Patent No. 6,373,346), Bosch et al. (U.S. Patent No. 6,130,562) and Inoue et al. (U.S. Patent No. 6,975,813), and further in view of Kenny (U.S. Patent No. 6,654,565). Claims 13 – 17 were rejected under 35 USC § 103(a) as being unpatentable over Kobayashi (U.S. Patent No. 6,373,346), Bosch et al. (U.S. Patent No. 6,130,562) and Inoue et al. (U.S. Patent No.6,975,813), and Kenny (U.S. Patent No. 6,654,565), and further in view of Diaz et al. (U.S. Patent No. 6,822,987). Applicants respectfully traverse these additional rejections.

Because these rejections are also based on the combination of Kobayashi, Bosch and Inoue, applicants submit that the combinations of references used in these rejections also do not teach or suggest all of the claimed limitations for the same reasons discussed above. Thus, applicants submit that claims 4-6 and 9-17 are patentable for the same reasons discussed above as well as for the additional limitations recited in these claims. Accordingly, applicants request that these additional rejections under 35 U.S.C. 103 be withdrawn.

*Conclusion*

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (603-668-6560) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-2121.

Respectfully submitted,

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